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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,436	KADOWAKI, YUKIO	
	Examiner	Art Unit	
	MICHAEL J. DIGIOVANNI	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 16-23* is/are rejected.

7)☒ Claim(s) *10-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *28 December 2005, 10 May 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Objections

A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

Claim 22 is objected to because of the following informalities: page 88 lines 4-5 of the claim recites “or the second transmission circuit" when it appears in view of claim 23 and the specification to be intended to recite "or the first transmission circuit". For the purposes of examination it is assumed to be “or the first transmission circuit”. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9 and 16-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujii (US 2006/0280112).

Regarding claim 1, Fujii discloses a serial communication device comprising a first transmission/reception circuit (fig. 20 item 2002) and at least one second transmission/reception circuit (fig. 20 item 2003) connected to the first transmission/reception circuit by a transmission path (fig. 20 item 2004) for performing serial communication by half-duplex communication between the first transmission/reception circuit and the second transmission/reception circuit (par. 125), wherein the first transmission/reception circuit outputs a serial data signal DATA (fig. 22 signal So51) to the transmission path, said serial data signal DATA being generated by superposing a first superposition pulse having a second level on a portion of a clock signal input from outside having a first level according to binary first transmission data to be output to the second transmission/reception circuit, said clock signal being a binary signal, said second level being reciprocal to said first level (fig. 22 where SDo51 is equivalent to binary first transmission data and So51 is equivalent to a signal with pulses superposed on clock signal S55); and the second transmission/reception circuit superposes a second superposition pulse having the first level on a portion of the serial data signal DATA input from the transmission path according to binary second transmission data to be output to the first transmission/reception circuit, said portion corresponding to a duration of the clock signal having the second level (fig. 27 where SDo52 is equivalent to binary second transmission data and So52 is equivalent to a signal with pulses superposed on a data signal Si52 received from the transmission path as stated in par. 151).

Regarding claim 2, Fujii discloses the serial communication device as claimed in claim 1, wherein the first transmission/reception circuit comprises: a first transmission circuit that superposes the first superposition pulse on the portion of the clock signal having the first level, and outputs the serial data signal DATA to the transmission path (fig. 20 item 2011); and a first reception circuit that extracts the second superposition pulse from the serial data signal DATA to extract the second transmission data (fig. 20 item 2012).

Regarding claim 3, Fujii discloses the serial communication device as claimed in claim 1, wherein the second transmission/reception circuit comprises: a second transmission circuit that superposes the second superposition pulse on the portion of the serial data signal DATA corresponding to the duration of the clock signal having the second level and transmits a resulting signal to the transmission path (fig. 20 item 2013); and a second reception circuit that extracts the first superposition pulse from the serial data signal DATA input from the first transmission/reception circuit to extract the second transmission data (fig. 20 item 2014).

Regarding claim 4, Fujii discloses the serial communication device as claimed in claim 2, wherein the first transmission circuit superposes the first superposition pulse having the second level and a pulse width T1 on the portion of the clock signal having the first level and a pulse width T3 starting from a predetermined starting point after a time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA (fig. 22 where T51 is equivalent to T1, T52 is equivalent to T2, and T53 is equivalent to T3), or the second transmission circuit

indicates another one of the two levels of one bit data in the serial data signal DATA when the first superposition pulse is absent after the time period T2 elapses from the starting point (fig. 22 where it can be seen that when a one is indicated in SDo51, a pulse is present in So51; and when a zero is indicated in SDo51, no pulse is present in So51); and the first transmission circuit generates and outputs the serial data signal DATA one bit by one bit consecutively to perform serial communication so that the pulse width T1, the pulse width T3, and the time period T2 satisfy: T1<T2<T3, and (T1+T2)<T3 (fig. 22 where So51 can be seen to output the data from SDo51 sequentially with T51<T52<T53 and (T51+T52)<T53).

Regarding claim 5, Fujii discloses the serial communication device as claimed in claim 3, wherein the second transmission circuit superposes the second superposition pulse having the first level and a pulse width T1 on the portion of the serial data signal DATA having the second level corresponding to the duration of the clock signal having the second level and a pulse width T3 starting from a predetermined starting point after the time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA (Fig. 27 where T51 is equivalent to T1, T52 is equivalent to T2, and T53 is equivalent to T3), or the second transmission circuit indicates another one of the two levels of one bit data in the serial data signal DATA when the second superposition pulse is absent after the time period T2 elapses from the starting point (fig. 27 where it can be seen that when a one is indicated in SDo52, a pulse is present in So52; and when a zero is indicated in SDo52, no pulse is present in So52); and the second transmission circuit generates and outputs the serial data signal

DATA one bit by one bit consecutively to perform serial communication so that the pulse width T1, the pulse width T3, and the time period T2 satisfy: T1<T2<T3, and (T1+T2)<T3 (fig. 27 where So52 can be seen to output the data from SDo52 sequentially with T51<T52<T53 and (T51+T52)<T53).

Regarding claim 6, Fujii discloses the serial communication device as claimed in claim 4, wherein the first transmission circuit comprises: a first T2 delay circuit that delays the clock signal by the time period T2 and outputs said delayed signal (fig. 21 item 2021 described in par. 130); a first T1 delay circuit that delays the output signal from the first T2 delay circuit by a time period T1 and outputs said delayed signal (fig. 21 item 2022 described in par. 130); a first superposition pulse generation circuit that generates the first superposition pulse having the pulse width T1 from the output signal from the first T2 delay circuit and the output signal from the first T1 delay circuit (fig. 21 item 2023 described in par. 130); and a first output signal generation circuit that superposes the first superposition pulse from the first superposition pulse generation circuit to the clock signal according to the first transmission data, and generates data equaling to one bit sequentially to generate the serial data signal DATA and to transmit the serial data signal DATA to the transmission path (fig. 21 item 2025 described in par. 130).

Regarding claim 7, Fujii discloses the serial communication device as claimed in claim 4, wherein the first reception circuit comprises: a first T4 delay circuit that delays the received serial data signal DATA by a time period T4 equaling to or greater than (T1+T2), and outputs said delayed signal (fig. 23 item 2032 described in par. 138); a

first input signal delay circuit that delays the output signal from the first T4 delay circuit by a predetermined time period and outputs said delayed signal (fig. 23 DEF12 where in fig. 24 it can be seen that the only difference between S19 and S20 is a delay, S19 being a result of the output of item 2032); and a first data extraction circuit that extracts the second transmission data from the received serial data signal DATA and the output signal from the first input signal delay circuit, and outputs the extracted signal (fig. 23 item 2034 described in par. 138).

Regarding claim 8, Fujii discloses the serial communication device as claimed in claim 5, wherein the second reception circuit comprises: a second T4 delay circuit that delays the received serial data signal DATA by the time period T4 equaling to or greater than (T1+T2), and outputs said delayed signal (fig. 26 items 2041 and 2042 described in par. 152); a second input signal delay circuit that delays the output signal from the second T4 delay circuit by a predetermined time period and outputs said delayed signal (fig. 26 DEF22); and a second data extraction circuit that extracts the first transmission data from the received serial data signal DATA and the output signal from the second input signal delay circuit, and outputs the extracted signal (fig. 26 item 2044 described in par. 152).

Regarding claim 9, Fujii discloses the serial communication device as claimed in claim 5, wherein the second transmission circuit comprises: a second T2 delay circuit that delays the received serial data signal DATA by the time period T2 and outputs said delayed signal (fig. 26 item 2042 as it can be seen in fig. 27 that the difference between S31 and S32 is the delay T52); a second T1 delay circuit that delays the output signal

from the second T2 delay circuit by a time period T1 and outputs said delayed signal (fig. 26 item 2051 as it can be seen in fig. 27 that the difference between S32 and S33 is the delay T51); a second superposition pulse generation circuit that generates the second superposition pulse having the pulse width T1 from the output signal from the second T2 delay circuit and the output signal from the second T1 delay circuit (fig. 26 item 2052 described in par. 154); and a second output signal generation circuit that superposes, according to the second transmission data, the second superposition pulse output from the second superposition pulse generation circuit to the portion of the received serial data signal DATA corresponding to the duration of the clock signal having the second level, and generates data equaling to one bit sequentially to generate the serial data signal DATA and to transmit the serial data signal DATA to the transmission path (fig. 26 item 2053 described in par. 154).

Regarding claim 16, Fujii discloses a serial communication method of a serial communication device that includes a first transmission/reception circuit (fig. 20 item 2002) and at least one second transmission/reception circuit (fig. 20 item 2003) connected with the first transmission/reception circuit in a transmission path (fig. 20 item 2004), and performs serial communication by half-duplex communication between the first transmission/reception circuit and the second transmission/reception circuit (par. 125), said method comprising the steps of: superposing a first superposition pulse having a second level on a portion of a clock signal input from outside having a first level according to binary first transmission data to be output to the second transmission/reception circuit, outputting a resulting serial data signal DATA (fig. 22

signal So51) to the transmission path, said clock signal being a binary signal, said second level being reciprocal to said first level (fig. 22 where SDo51 is equivalent to binary first transmission data and So51 is equivalent to a signal with pulses superposed on clock signal S55); and superposing a second superposition pulse having the first level on a portion of the serial data signal DATA input from the transmission path corresponding to a duration of the clock signal having the second level according to binary second transmission data to be output to the first transmission/reception circuit (fig. 27 where SDo52 is equivalent to binary second transmission data and So52 is equivalent to a signal with pulses superposed on a data signal Si52 received from the transmission path as stated in par. 151).

Regarding claim 17, Fujii discloses the method as claimed in claim 16, wherein the step of superposing the first superposition pulse includes the steps of: superposing the first superposition pulse having the second level and a pulse width T1 on the portion of the clock signal having the first level and a pulse width T3 starting from a predetermined starting point after a time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA (fig. 22 where T51 is equivalent to T1, T52 is equivalent to T2, and T53 is equivalent to T3), or indicating another one of the two levels of one bit data in the serial data signal DATA when the first superposition pulse is absent after the time period T2 elapses from the starting point (fig. 22 where it can be seen that when a one is indicated in SDo51, a pulse is present in So51; and when a zero is indicated in SDo51, no pulse is present in So51); and generating and outputting the serial data signal DATA one bit by one bit

consecutively to perform serial communication so that the pulse width T1, the pulse width T3, and the time period T2 satisfy: T1<T2<T3, and (T1+T2)<T3 (fig. 22 where So51 can be seen to output the data from SDo51 sequentially with T51<T52<T53 and (T51+T52)<T53).

Regarding claim 18, Fujii discloses the method as claimed in claim 16, wherein the step of superposing the second superposition pulse includes the steps of: superposing the second superposition pulse having the first level and a pulse width T1 on the portion of the serial data signal DATA having the second level corresponding to the duration of the clock signal having the second level and a pulse width T3 starting from a predetermined starting point after the time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA (Fig. 27 where T51 is equivalent to T1, T52 is equivalent to T2, and T53 is equivalent to T3), or indicating another one of the two levels of one bit data in the serial data signal DATA when the second superposition pulse is absent after the time period T2 elapses from the starting point (fig. 27 where it can be seen that when a one is indicated in SDo52, a pulse is present in So52; and when a zero is indicated in SDo52, no pulse is present in So52); and generating and outputting the serial data signal DATA one bit by one bit consecutively to perform serial communication so that the pulse width T1, the pulse width T3, and the time period T2 satisfy: T1<T2<T3, and (T1+T2)<T3 (fig. 27 where So52 can be seen to output the data from SDo52 sequentially with T51<T52<T53 and (T51+T52)<T53).

Regarding claim 19, Fujii discloses a communication system comprising a serial communication device that includes a first transmission/reception circuit (fig. 20 item 2002) connected to a host device and at least one second transmission/reception circuit (fig. 20 item 2003) connected corresponding to slave devices able to communicate with the host device, and performs serial communication by half-duplex communication between the first transmission/reception circuit and the second transmission/reception circuit (par. 125), said first transmission/reception circuit and said second transmission/reception circuit being connected with each other in a transmission path (fig. 20 item 2004), wherein the first transmission/reception circuit of the serial communication device outputs a serial data signal DATA (fig. 22 signal So51) to the second transmission/reception circuit via the transmission path, said serial data signal DATA being generated by superposing a first superposition pulse having a second level on a portion of a clock signal input from the host device having a first level according to binary first transmission data to be transmitted from the host device to the slave device, said clock signal being a binary signal, said second level being reciprocal to said first level (fig. 22 where SDo51 is equivalent to binary first transmission data and So51 is equivalent to a signal with pulses superposed on clock signal S55); and the second transmission/reception circuit of the serial communication device superposes a second superposition pulse having the first level on a portion of the serial data signal DATA input from the first transmission/reception circuit transmission path according to binary second transmission data to be output from the corresponding slave device to the host device, said portion corresponding to a duration of the clock signal having the second

level (fig. 27 where SDo52 is equivalent to binary second transmission data and So52 is equivalent to a signal with pulses superposed on a data signal Si52 received from the transmission path as stated in par. 151).

Regarding claim 20, Fujii discloses the communication system as claimed in claim 19, wherein the first transmission/reception circuit comprises: a first transmission circuit that superposes the first superposition pulse on the portion of the clock signal having the first level, and outputs the serial data signal DATA to the transmission path (fig. 20 item 2011); and a first reception circuit that extracts the second superposition pulse from the serial data signal DATA to extract the second transmission data (fig. 20 item 2012).

Regarding claim 21, Fujii discloses the communication system as claimed in claim 19, wherein the second transmission/reception circuit comprises: a second transmission circuit that superposes the second superposition pulse on the portion of the serial data signal DATA corresponding to the duration of the clock signal having the second level and transmits a resulting signal to the transmission path (fig. 20 item 2013); and a second reception circuit that extracts the first superposition pulse from the serial data signal DATA input from the first transmission/reception circuit to extract the second transmission data (fig. 20 item 2014).

Regarding claim 22, Fujii discloses the communication system as claimed in claim 20, wherein the first transmission circuit superposes the first superposition pulse having the second level and a pulse width T1 on the portion of the clock signal having the first level and a pulse width T3 starting from a predetermined starting point after a

time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA (fig. 22 where T51 is equivalent to T1, T52 is equivalent to T2, and T53 is equivalent to T3), or the second transmission circuit indicates another one of the two levels of one bit data in the serial data signal DATA when the first superposition pulse is absent after the time period T2 elapses from the starting point (fig. 22 where it can be seen that when a one is indicated in SDo51, a pulse is present in So51; and when a zero is indicated in SDo51, no pulse is present in So51); and the first transmission circuit generates and outputs the serial data signal DATA one bit by one bit consecutively to perform serial communication so that the pulse width T1, the pulse width T3, and the time period T2 satisfy: T1<T2<T3, and (T1+T2)<T3 (fig. 22 where So51 can be seen to output the data from SDo51 sequentially with T51<T52<T53 and (T51+T52)<T53).

Regarding claim 23, Fujii discloses the communication system as claimed in claim 21, wherein the second transmission circuit superposes the second superposition pulse having the first level and a pulse width T1 to the portion of the serial data signal DATA having the second level corresponding to the duration of the clock signal having the second level and a pulse width T3 starting from a predetermined starting point after the time period T2 elapses from the starting point to indicate one of two levels of one bit data in the serial data signal DATA (Fig. 27 where T51 is equivalent to T1, T52 is equivalent to T2, and T53 is equivalent to T3), or the second transmission circuit indicates another one of the two levels of one bit data in the serial data signal DATA when the second superposition pulse is absent after the time period T2 elapses from

the starting point (fig. 27 where it can be seen that when a one is indicated in SDo52, a pulse is present in So52; and when a zero is indicated in SDo52, no pulse is present in So52); and the second transmission circuit generates and outputs the serial data signal DATA one bit by one bit consecutively to perform serial communication so that the pulse width T1, the pulse width T3, and the time period T2 satisfy: T1<T2<T3, and (T1+T2)<T3 (fig. 27 where So52 can be seen to output the data from SDo52 sequentially with T51<T52<T53 and (T51+T52)<T53).

Allowable Subject Matter

Claims 10-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 10-15, Fujii discloses the serial communication system of claims 6 and 9, but does not disclose high impedance states or shorting of pull resistances.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL J. DIGIOVANNI whose telephone number is (571)270-7508. The examiner can normally be reached on Monday-Thursday 7:30AM-5:00PM and every other Friday from 7:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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